Chapter 6
Am8212 INPUT/OUTPUT PORT

The Am8212 is a general purpose device that provides TTL compatible, parallel 8-bit interface logic with high fan-out for a wide variety of applications in typical microprocessor systems. It may be used as a bus driver, an input port, an output port, or in other applications such as gating interrupt vectors to the Data Bus.

This device has an output high signal level of 3.65 volts or greater, insuring compatibility with virtually every microprocessor available. An input low current load on the data lines of 0.25 mA and a high output sink current drive on the data lines of 15 mA makes the part very flexible as an interface element to microprocessor Data Busses.

FUNCTIONAL DESCRIPTION

The logic diagram for the Am8212 is shown in Figure 6-1. It shows 8-bit parallel latch and driver circuits, plus interrupt request and enable control logic.

The 8-bit parallel data logic consists of eight D-type flip-flops each of which has a noninverting 3-state buffer on the Q outputs. This combination allows data to be transferred from external logic into the microcomputer system or from the microcomputer system to external logic.

In order to transfer data from external logic to the microcomputer system, information can be input to the D-type flip-flops at any time, whether or not the Am8212 device has been selected by the microprocessor. When the microprocessor selects the device, internal logic causes the contents of the flip-flops to be output by enabling the eight 3-state buffers on the flip-flop output lines.

The interrupt logic is designed to create an interrupt request during the time interval between external logic strobing data into the latches and the microprocessor reading this data.

When the Am8212 device is being used to transfer data from a microcomputer system to external logic, the microprocessor provides the data input and device select logic causes input data to be strobed into the flip-flops. Simultaneously the 3-state buffers on the flip-flop outputs are enabled so that external logic is able to read data off the output lines.

Am8212 INTERFACE SIGNALS

Figure 6-2 shows the Connection Diagram for the Am8212.

Input

Data Input (DI0 - DI7, Input)
These are the eight Data Input signals to the D-type flip-flops.

Clear ($\overline{CLR}$, Input)
$\overline{CLR}$ resets all of the data flip-flops when input low, and sets the interrupt request signal $\overline{INT}$ high.

Device Select ($\overline{DS1}$ and DS2, Input)
These signals are used to select the Am8212 for an active operation. $\overline{DS1}$ must be low and DS2 must be high for selection. The consequences of selecting the Am8212 are a function of the mode in which the device is operating.

Mode Select (MD, Input)
The MD input determines whether the unit will be operated in Input or Output mode.

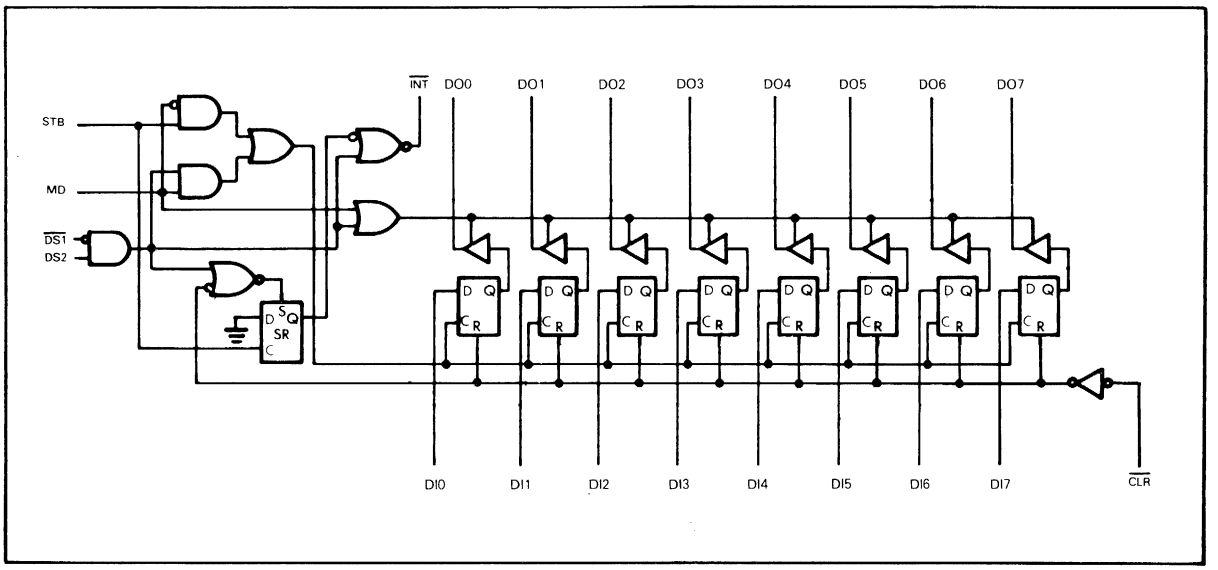

FIGURE 6-1 Am8212 LOGIC DIAGRAM

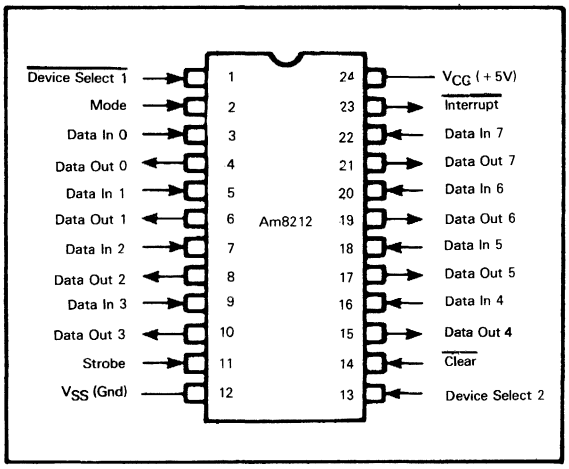

FIGURE 6-2 Am8212 CONNECTION DIAGRAM

When MD is low, the Am8212 is operating in Input mode. In this mode device select logic enables output on the DO0-DO7 pins while separate logic strobes data into the Am8212, irrespective of whether the device has been selected.

When MD is high, the Am8212 is operating in Output Mode. Now device select logic simultaneously strobes data into the flip-flops and enables data out.

Strobe (STB, Input)

Strobe is an input control signal which is active in Input Mode only. External logic uses this signal in order to strobe data into the flip-flops. This signal also contributes to the logic which determines the level of the interrupt request signal INT.

Output

Data Output (DO0 - DO7, Output)

DO0 through DO7 are the eight data output signals from the 3-state buffers.

Interrupt Request ($\overline{INT}$, Output)

This is the output signal used to request interrupt service from the microprocessor.

OPERATING MODES

The simplest way of understanding Am8212 logic is to initially ignore the interrupt section and examine the 8-bit parallel data path when the device is operating in Input or Output mode.

There are two important signals created within the Am8212: the D-type flip-flop clock input and the output buffer enable. Logic equations for these two signals are as follows:

$C = (\overline{MD} \cdot STB) + (MD \cdot (\overline{DS1} \cdot DS2))$ Clock equation

$EN = MD + \overline{DS1} \cdot DS2$ Output buffer enable equation

Output Mode

Output Mode operation is selected by the MD control being input high. MD high forces the first term of the clock equation to remain permanently low thereby negating the STB signal. The D-type flip-flop clock input will now follow the device select. Simultaneously, MD high permanently enables EN, the output buffer enable control. Thus, flip-flops will be enabled. The flip-flop inputs will be sampled when the clock signal is high, which occurs when the device is selected.

Output Mode acquires its name from the fact that this use of the Am8212 will normally occur when the DI pins are connected to the microcomputer system Data Bus while the DO pins are connected to external logic. Thus an output or write instruction that selects the Am8212 will cause select logic to go true. This permits the data to flow through the flip-flops and out to external logic.

If external logic is connected to the DI pins in Output Mode, while the microcomputer system Data Bus is connected to the DO pins, then a memory read or input instruction that selects the Am8212 will cause the microcomputer system to read whatever data happens to be instantaneously present at the DI pins when the Am8212 is selected.

Input Mode

Input Mode operation is characterized by the MD control signal being input low. Referring to the flip-flop clock signal equation, a low MD input will force the second term of the clock signal equation to be inactive. Now the clock signal will follow the strobe input (STB). Irrespective of whether the Am8212 is selected or not, external logic may load data into the flip-flops by pulsing STB high while data is stable on the DI pins. The output buffer enable signal, on the other hand, must rely on device select logic for a high input, since in the first term of the buffer enable equation MD will always be low. Thus, the outputs of the flip-flops will not be available at the DO pins until the Am8212 has been selected by an input or read instruction.

Input Mode gets its name from the fact that in this mode external logic is normally connected to the DI pins while the DO pins connect to the system Data Bus. Clocking data into the flip-flops via the STB signal and enabling the outputs onto the Data Bus via the device select logic are asynchronous events. External logic can input data to the D-type flip-flops at any time and the microprocessor can subsequently read the data.

Note that nothing in the logic of the device prevents the microprocessor from connecting to the DI inputs in Input Mode, while external logic connects to the DO outputs. In this case, device select logic must now create the STB signal, while external logic must input the device select signals, $\overline{DS1}$ and DS2. In this configuration, the Am8212 is operating as a buffered and strobed output port.

INTERRUPT LOGIC

Interrupt logic associated with the Am8212 is aimed at providing Input Mode handshaking controls. Timing is illustrated in Figure 6-3.

With its D input tied to ground, the STB pulse will force the $\overline{INT}$ output low as long as the SR flip-flop is not being

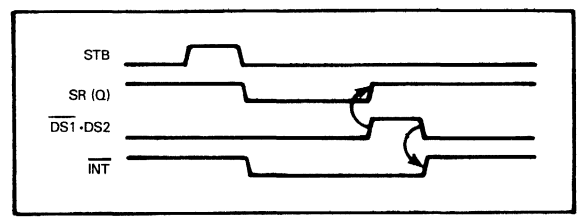

FIGURE 6-3 INTERRUPT LOGIC

clamped by the CLR input. $\overline{INT}$ will remain low until device select logic has completed a select high pulse. Thus, the $\overline{INT}$ signal remains low for the time interval between external logic strobing data into the D-type flip-flops and the microprocessor reading this data. Table 6-1 summarizes the condition of the INT output as a function of the possible inputs. SR is the internal Service Request Latch.

In the simplest case the $\overline{INT}$ output of the Am8212 device will be connected to the microprocessor's interrupt request logic. As soon as external logic strobes data into the D-type flip-flops, an interrupt request will occur. The microprocessor can enter an interrupt service routine which reads the contents of the flip-flops.

Alternatively, the $\overline{INT}$ output may be used as a handshaking signal to external logic. When external logic strobes data into the D-type flip-flops, $\overline{INT}$ is immediately output low. External logic may use the subsequent low-to-high transition of $\overline{INT}$ as an acknowledge that the microprocessor has read the contents of the Am8212 device, indicating that the external logic is free to transmit new data to the DI pins.

TABLE 6-1 $\overline{INT}$ SIGNAL LOGIC

CLR	$\overline{(DS1 \cdot DS2)}$	STB	SR	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

APPLICATIONS

Shown here are several examples of the use of the Am8212 8-bit I/O Port. These are largely illustrative in that many of its functions can now be implemented in Low-power Schottky.

Unidirectional Bus Buffer

Figure 6-4 illustrates the Am8212 device being used as a simple bus buffer.

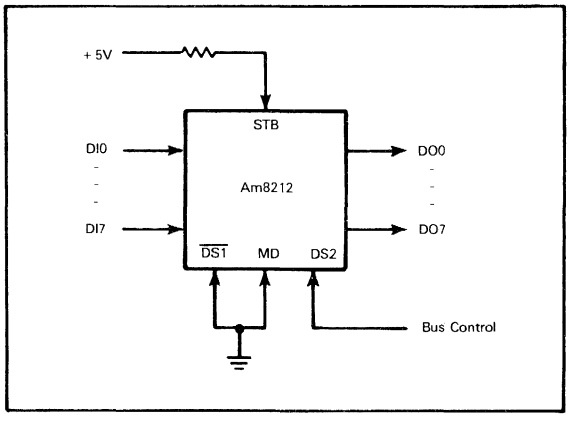

FIGURE 6-4 AN Am8212 CONFIGURED AS A BUS BUFFER

In this case, the device is operated in Input Mode, since device select logic enables or disables the buffers on the outputs. Since latching in the Input Mode is not required, the STB signal is tied high. Thus, data entering the DI pins will appear at the output. MD is shown tied to ground, which is required for Input Mode. $\overline{DS1}$ is also tied to ground. Select logic is now based on DS2. Whenever a high input occurs at DS2, data entering via the DI pins will flow through to the DO pins. Any signal will do — a data line, an address line or a control signal. As soon as DS2 receives a low input, the DO pins will enter their high impedance state. Newer microcomputer system designs would make use of the Am74LS241 for the application. This results in lower cost and lower power and replaces a 24-pin with a 20-pin device.

Bidirectional Buffer/Bus Driver

The Am8212 is easily configured as a bidirectional bus driver. In the high impedance state, the bidirectional bus driver configuration provides very low loading on one side of the bus, while maintaining high fan-out capability on the other side.

Figure 6-5 shows two Am8212 circuits connected in parallel as a bidirectional buffer/bus driver. The $\overline{STB}$, MD and DS control signal connections are similar to the unidirectional bus driver; however the $\overline{DS1}$ and DS2 control signals are selected so that the output of one is in the high impedance state when the other is in the active data transfer mode.

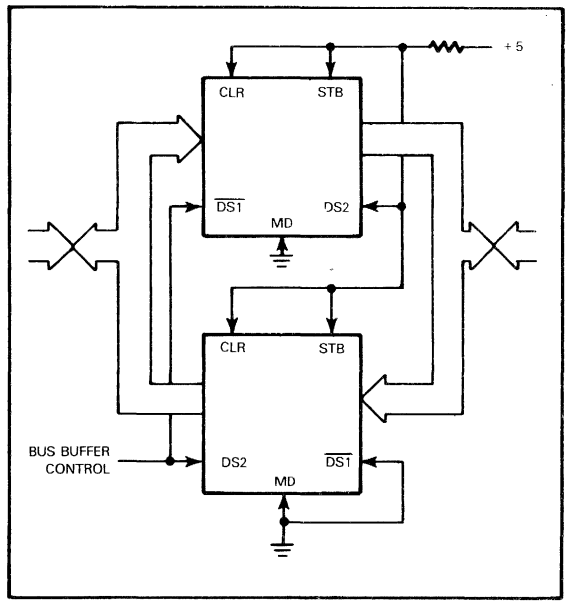

FIGURE 6-5 BIDIRECTIONAL BUS BUFFER

Again, the Low-power Schottky Am74LS241 would be a better choice for new designs in many applications.

Input Port

Two configurations for the Am8212 used as an input port, are shown in Figures 6-6 and 6-7.

In Figure 6-6 the Am8212 is connected as a port without latched inputs. The Interrupt signal is not used with this configuration because STB is permanently high.

Since MD is held low, the Am8212 is being operated in Input

Mode. However, STB is held high; therefore data arriving on the DI inputs from external logic will flow continuously into the flip-flops.

The device select signals, $\overline{DS1}$ and DS2, are used in an interesting way. Device address logic creates a single high signal in order to select the Am8212; this high signal is input at DS2. Simultaneously, the read pulse which will accompany an input or memory read instruction's execution is connected to $\overline{DS1}$. Thus the low read pulse accompanying device select will satisfy the device select logic to enable the output buffers.

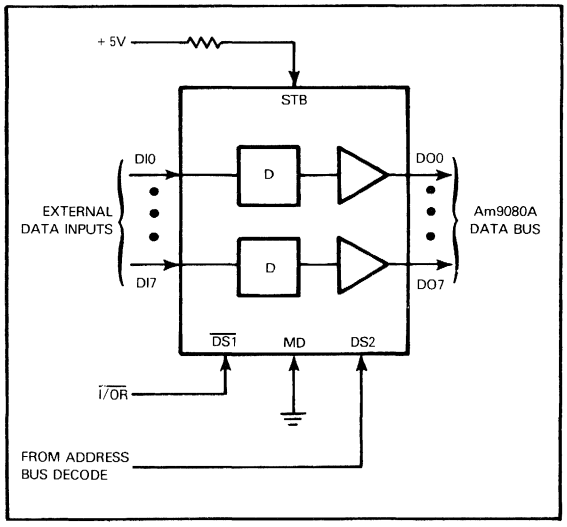

FIGURE 6-6 UNLATCHED INPUT PORT

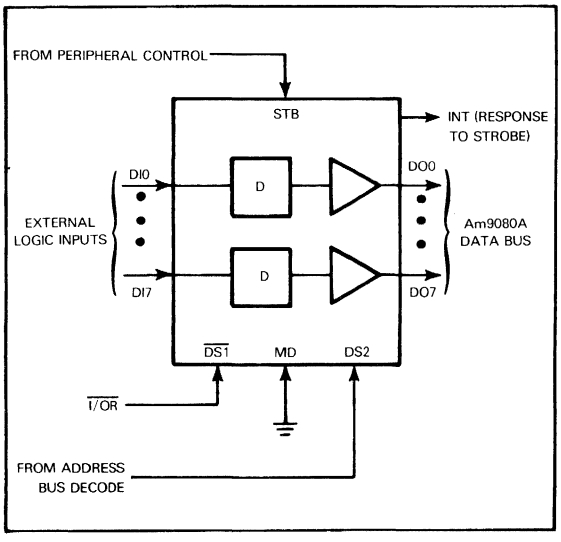

FIGURE 6-7 LATCHED INPUT PORT

The Figure 6-7 configuration shows the strobe signal STB connected to peripheral control logic which latches the input data and creates an interrupt request. Notice that STB determines the instant at which the latches accept data at the DI inputs. The DS signals determine when the latch outputs are connected to the Data Bus, and when they are in the high impedance state.

Output Port

Figure 6-8 shows the use of the Am8212 as an output port. Notice that MD is connected to +5V, creating Output Mode. $\overline{DS1}$ is connected to the microprocessor system $\overline{I/OW}$ signal, and STB can be used by the external peripheral circuit to acknowledge that information has been read by the peripheral device. In Output Mode the operation of STB does not affect the transfer of information from the input Data Bus to the latches or the data output of the Am8212; STB does activate the interrupt request to signal the CPU that the data transfer has been completed. The operation of $\overline{DS1}$ and DS2 will determine when information is read from the Data Bus into the Am8212. $\overline{DS1}$ is connected to the $\overline{I/OW}$ signal from the Am8228/8238 and DS2 is generated from the chip select logic connected to the Address Bus.

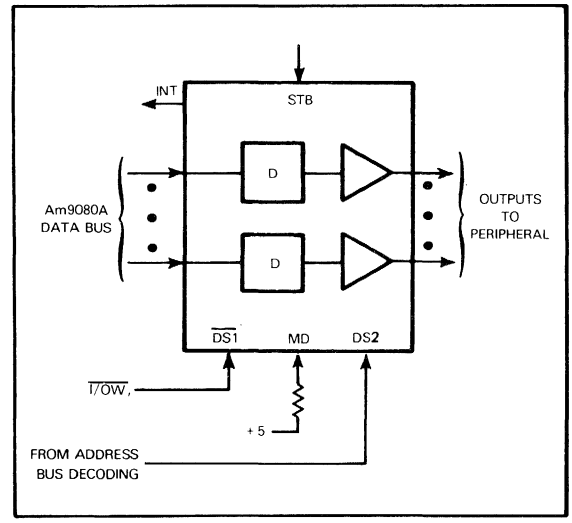

FIGURE 6-8 OUTPUT PORT

Status Latch

An Am8212 may be used as a latch to store the status signals that occur on the Am9080A Data Bus during the T1 clock period of each M1 machine cycle. When using the Am8212, rather than the Am8228/8238 System Controller, the status signal Stack will be present at the output of status latches for those applications that require it. Figure 6-9 shows a logical connection of the Am8212 as a status latch.

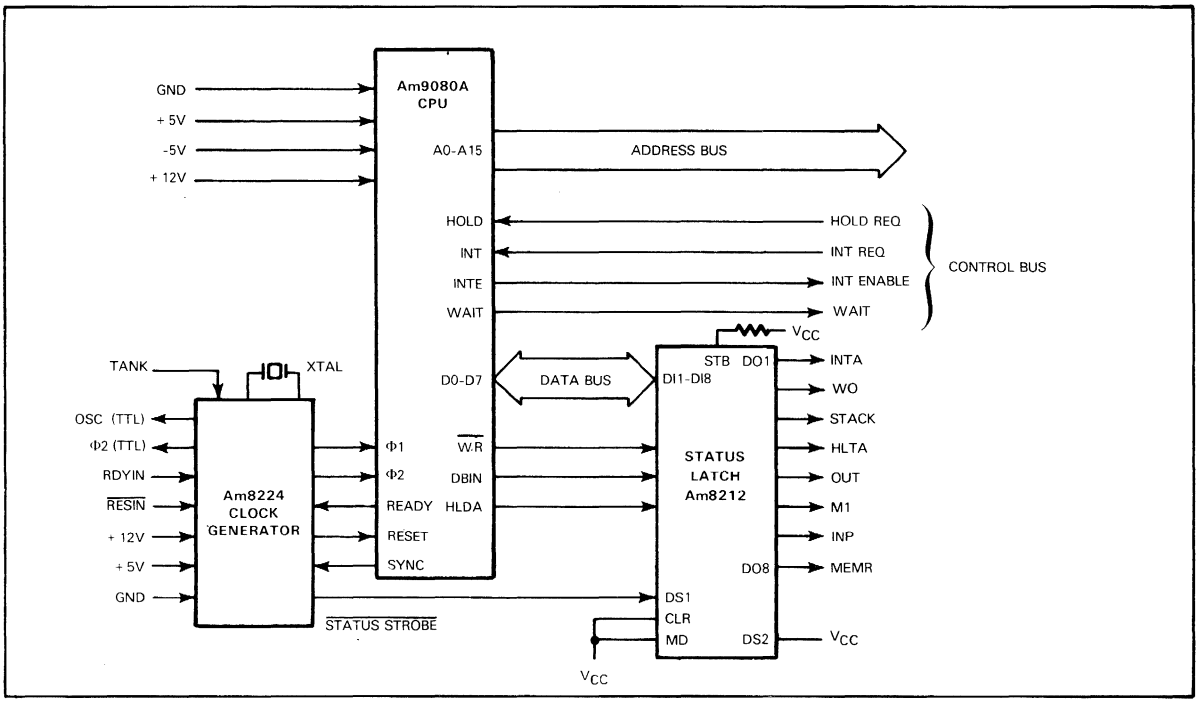

FIGURE 6-9 THE Am8212 USED AS A STATUS LATCH