



8212

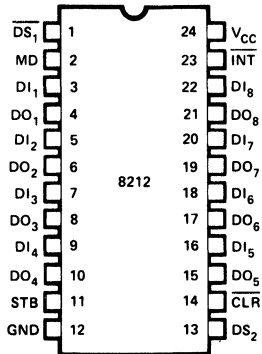
8-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25mA Max.
- Three State Outputs
- Outputs Sink 15mA
- 3.65V Output High Voltage for Direct Interface to 8008, 8080A, or 8085A CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

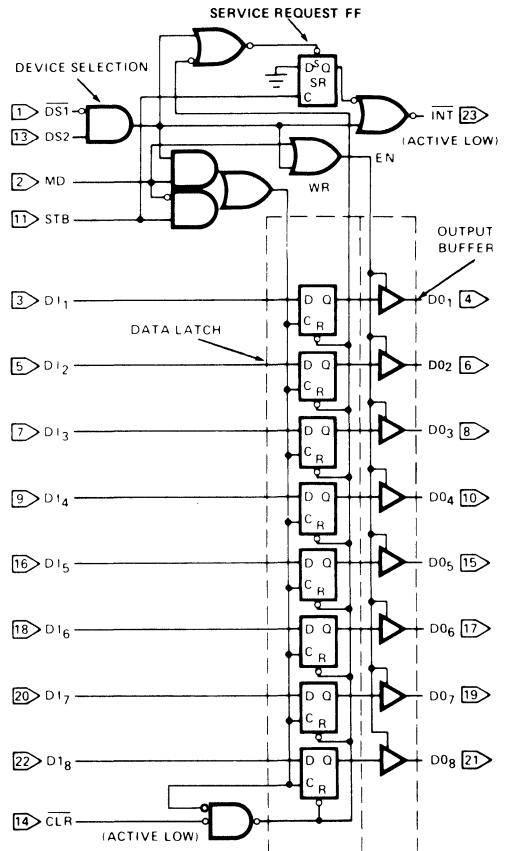
PIN CONFIGURATION



PIN NAMES

DI ₁ -DI ₈	DATA IN
DO ₁ -DO ₈	DATA OUT
DS ₁ -DS ₂	DEVICE SELECT
MD	MODE
STB	STROBE
INT	INTERRUPT (ACTIVE LOW)
CLR	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The latched data is cleared by an asynchronous reset input (CLR). (Note: Clock (C) Overrides Reset (CLR).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

The high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS1}$, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

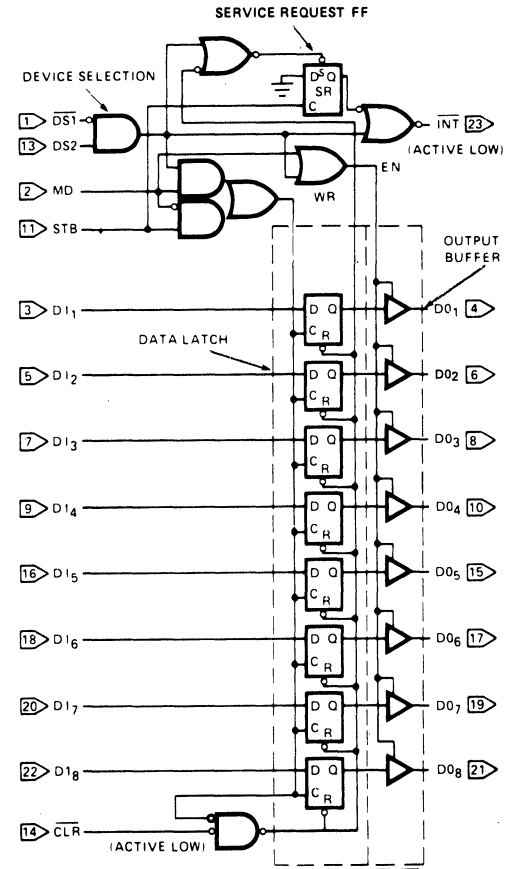
This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the CLR input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($DS1 \cdot DS2$). The output of the "NOR" gate (INT) is active low (interrupting state) for connection to active low input priority generating circuits.



STB	MD	(DS ₁ ·DS ₂)	DATA OUT EQUALS	CLR	(DS ₁ ·DS ₂)	STB	*SR	INT
0	0	0	3-STATE	0	0	0	1	1
1	0	0	3-STATE	0	1	0	1	0
0	1	0	DATA LATCH	1	1	0	0	0
1	1	0	DATA LATCH	1	1	0	1	1
0	0	1	DATA LATCH	1	0	0	1	1
1	0	1	DATA IN	1	1	0	1	1
0	1	1	DATA IN	1	1	1	0	0
1	1	1	DATA IN	1	1	1	1	0

*INTERNAL SR FLIP-FLOP
CLR - RESETS DATA LATCH
SETS SR FLIP-FLOP
(NO EFFECT ON OUTPUT BUFFER)

Applications of the 8212 — For Microcomputer Systems

- I Basic Schematic Symbol
- II Gated Buffer
- III Bi-Directional Bus Driver
- IV Interrupting Input Port

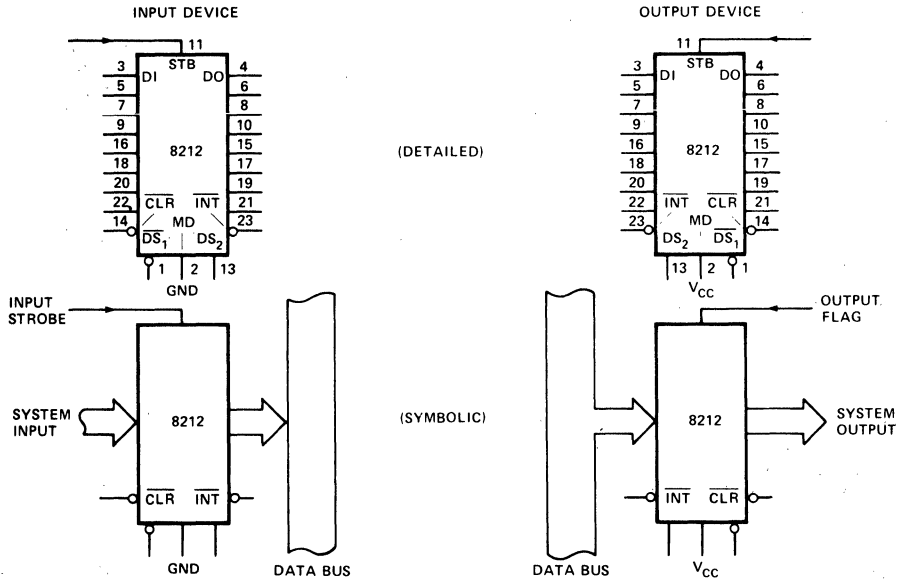
- V Interrupt Instruction Port
- VI Output Port
- VII 8080A Status Latch
- VIII 8085A Address Latch

1. Basic Schematic Symbols

Two examples of ways to draw the 8212 on system schematics — (1) the top being the detailed view showing pin numbers, and (2) the bottom being the symbolic view

showing the system input or output as a system bus (bus containing 8 parallel lines). The output to the data bus is symbolic in referencing 8 parallel lines.

BASIC SCHEMATIC SYMBOLS



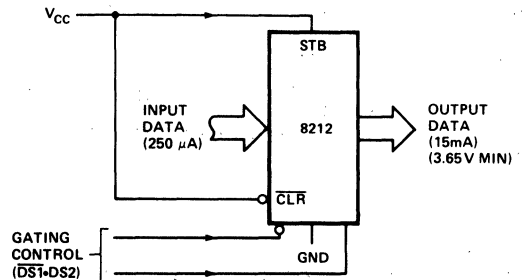
II. Gated Buffer (3-State)

The simplest use of the 8212 is that of a gated buffer. By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS1}$ and $\overline{DS2}$.

When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output. The input data load is 250 micro amps. The output data can sink 15 milli amps. The minimum high output is 3.65 volts.

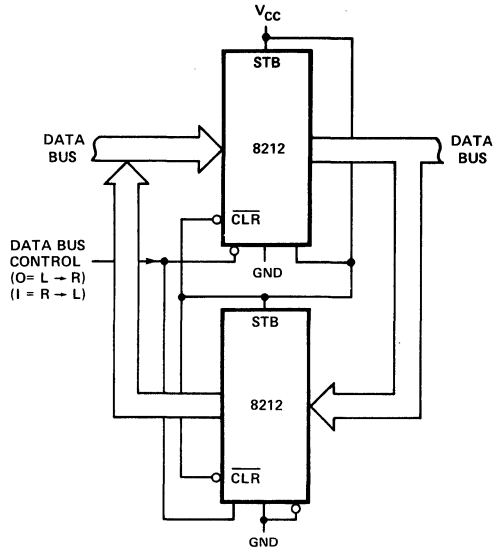
GATED BUFFER



III. Bi-Directional Bus Driver

A pair of 8212's wired (back-to-back) can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS1}$ on the first 8212 and to $DS2$ on the second. One device is active, and acting as a straight through buffer the other is in 3-state mode. This is a very useful circuit in small system design.

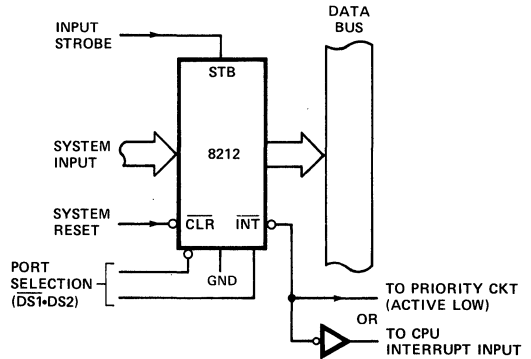
BI-DIRECTIONAL BUS DRIVER



IV. Interrupting Input Port

This use of an 8212 is that of a system input port that accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true — enabling the system input data onto the data bus.

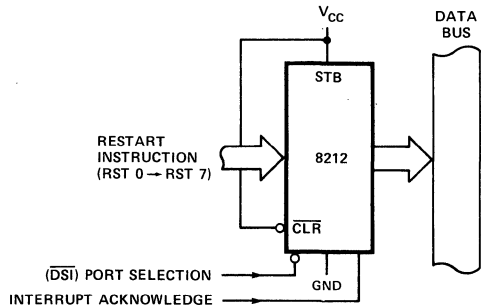
INTERRUPTING INPUT PORT



V. Interrupt Instruction Port

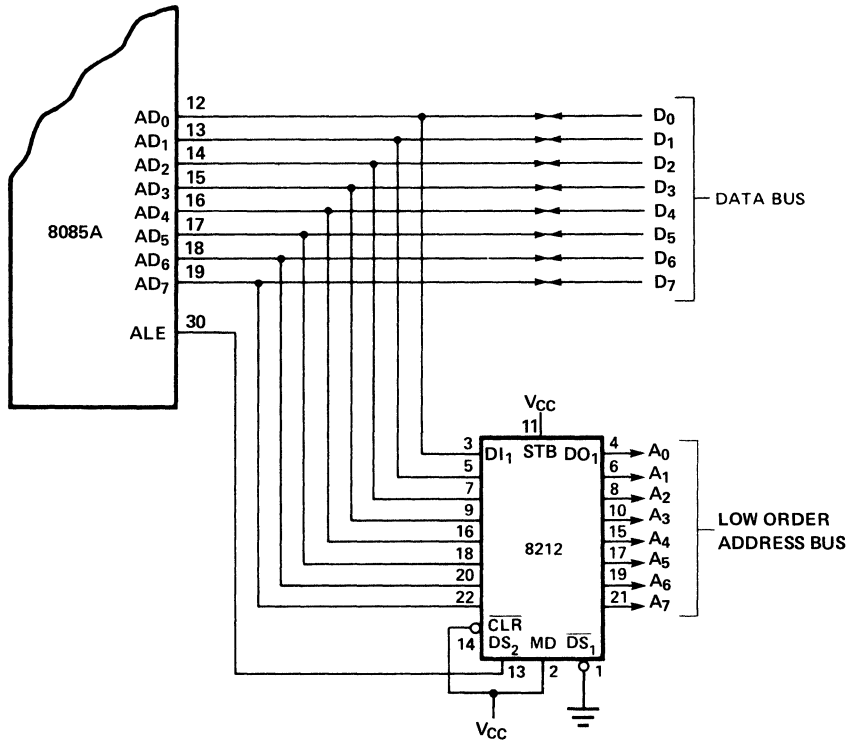
The 8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).

INTERRUPT INSTRUCTION PORT



VIII. 8085A Low-Order Address Latch

The 8085A microprocessor uses a multiplexed address/data bus that contains the low order 8-bits of address information during the first part of a machine cycle. The same bus contains data at a later time in the cycle. An address latch enable (ALE) signal is provided by the 8085A to be used by the 8212 to latch the address so that it may be available through the whole machine cycle. Note: In this configuration, the MODE input is tied high, keeping the 8212's output buffers turned on at all times.



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias Plastic	0°C to +70°C
Storage Temperature	-65°C to +160°C
All Output or Supply Voltages	-0.5 to +7 Volts
All Input Voltages	-1.0 to 5.5 Volts
Output Currents	100mA

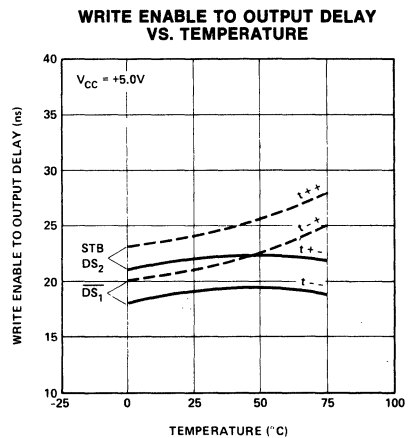
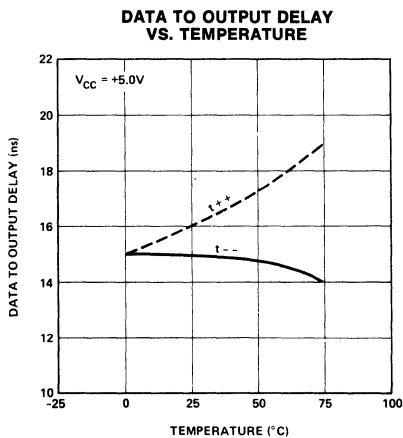
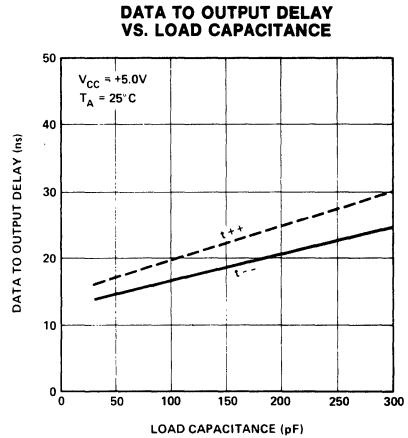
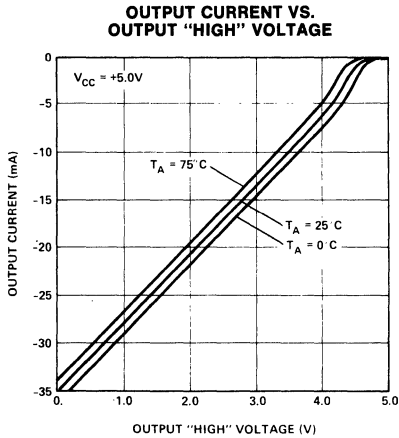
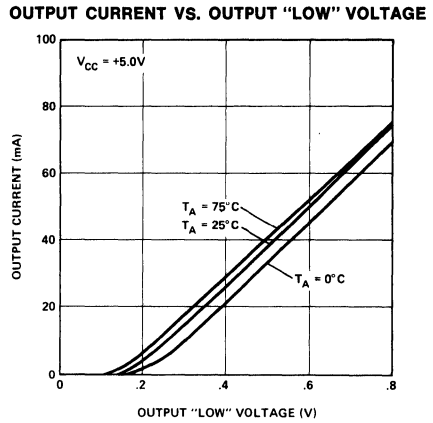
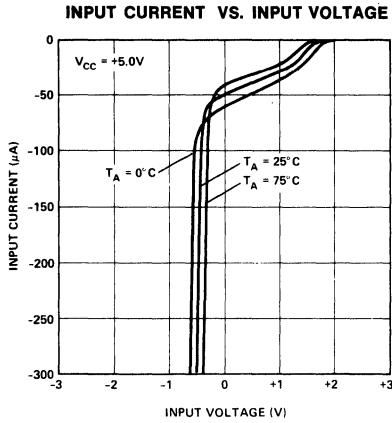
***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } +75^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I _F	Input Load Current, ACK, DS ₂ , CR, DI ₁ -DI ₈ Inputs			-.25	mA	V _F = .45V
I _F	Input Load Current MD Input			-.75	mA	V _F = .45V
I _F	Input Load Current DS ₁ Input			-1.0	mA	V _F = .45V
I _R	Input Leakage Current, ACK, DS, CR, DI ₁ -DI ₈ Inputs			10	μA	V _R ≤ V _{CC}
I _R	Input Leakage Current MO Input			30	μA	V _R ≤ V _{CC}
I _R	Input Leakage Current DS ₁ Input			40	μA	V _R ≤ V _{CC}
V _C	Input Forward Voltage Clamp			-1	V	I _C = -5mA
V _{IL}	Input "Low" Voltage			.85	V	
V _{IH}	Input "High" Voltage	2.0			V	
V _{OL}	Output "Low" Voltage			.45	V	I _{OL} = 15mA
V _{OH}	Output "High" Voltage	3.65	4.0		V	I _{OH} = -1mA
I _{SC}	Short Circuit Output Current	-15		-75	mA	V _O = 0V, V _{CC} = 5V
I _O	Output Leakage Current High Impedance State			20	μA	V _O = .45V/5.25V
I _{CC}	Power Supply Current		90	130	mA	

TYPICAL CHARACTERISTICS



A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
tpw	Pulse Width	30			ns	
tpD	Data to Output Delay			30	ns	Note 1
twe	Write Enable to Output Delay			40	ns	Note 1
tSET	Data Set Up Time	15			ns	
tH	Data Hold Time	20			ns	
tr	Reset to Output Delay			40	ns	Note 1
ts	Set to Output Delay			30	ns	Note 1
tE	Output Enable/Disable Time			45	ns	Note 1
tc	Clear to Output Delay			55	ns	Note 1

CAPACITANCE* $F = 1\text{MHz}$, $V_{BIAS} = 2.5V$, $V_{CC} = +5V$, $T_A = 25^\circ\text{C}$

Symbol	Test	Limits	
		Typ.	Max.
C _{IN}	DS ₁ MD Input Capacitance	9pF	12pF
C _{IN}	DS ₂ , CK, ACK, DI ₁ -DI ₈ Input Capacitance	5pF	9pF
C _{OUT}	DO ₁ -DO ₈ Output Capacitance	8pF	12pF

*This parameter is sampled and not 100% tested.

SWITCHING CHARACTERISTICS**Conditions of Test**

Input Pulse Amplitude = 2.5V
 Input Rise and Fall Times 5ns
 Between 1V and 2V Measurements made at 1.5V
 with 15mA and 30pF Test Load

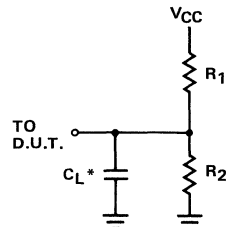
Note 1:

Test	C _L *	R ₁	R ₂
tpD, twe, tr, ts, tc	30pF	300Ω	600Ω
tE, ENABLE↑	30pF	10KΩ	1KΩ
tE, ENABLE↓	30pF	300Ω	600Ω
tE, DISABLE↑	5pF	300Ω	600Ω
tE, DISABLE↓	5pF	10KΩ	1KΩ

*Includes probe and jig capacitance.

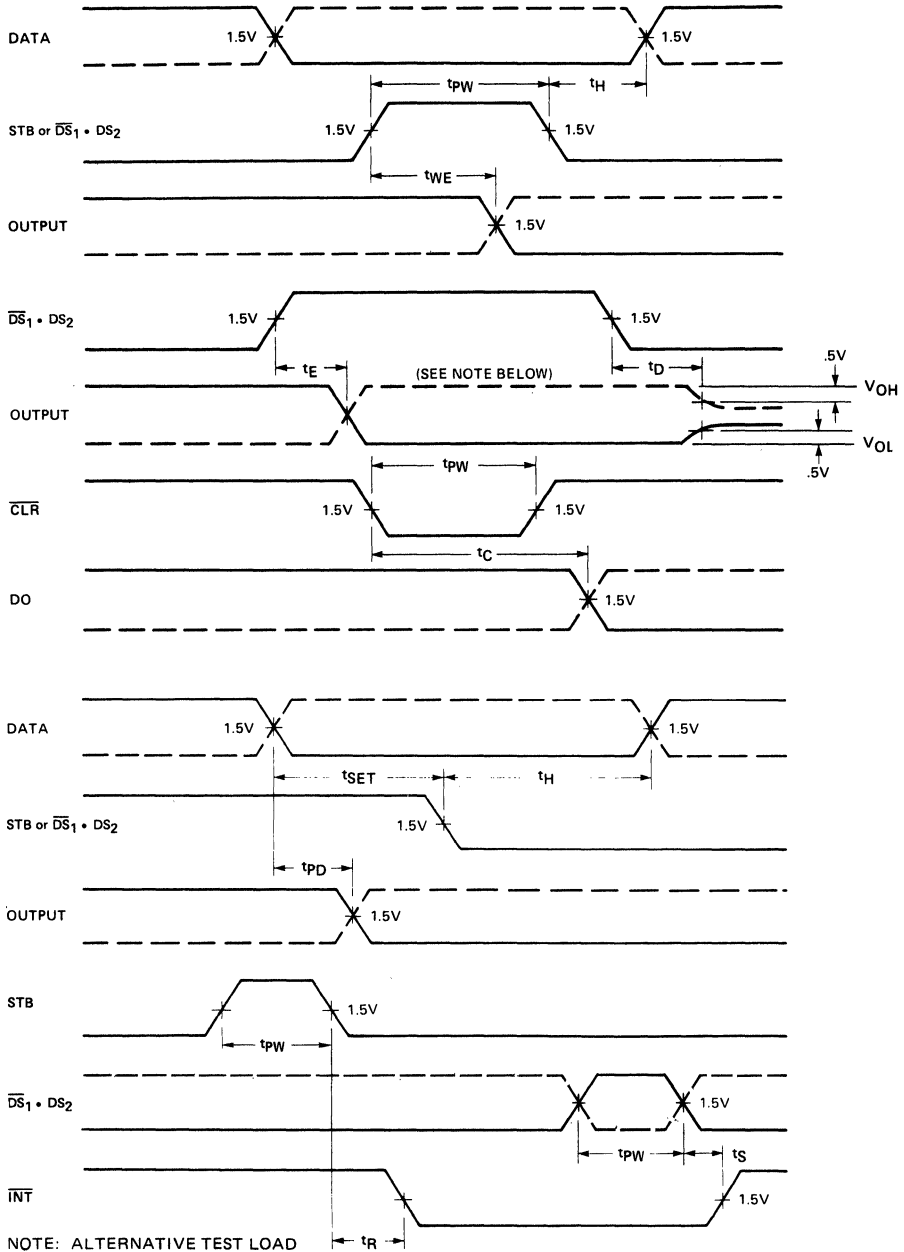
Test Load

15mA & 30pF



*INCLUDING JIG & PROBE CAPACITANCE

TIMING DIAGRAM



NOTE: ALTERNATIVE TEST LOAD

