M8212
8-BIT INPUT/OUTPUT PORT

MILITARY

- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current 0.25mA Max**
- **3-State Outputs**
- **Military Temperature Range -55° C to +125° C**
- **3.4V Output High Voltage for Direct Interface to M8080A CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches, and Multiplexers in Microcomputer Systems**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**
- **24-Pin Dual In-Line Package**

The Intel® M8212/M3212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

*Note: The specifications for the M3212 are identical with those for the M8212.

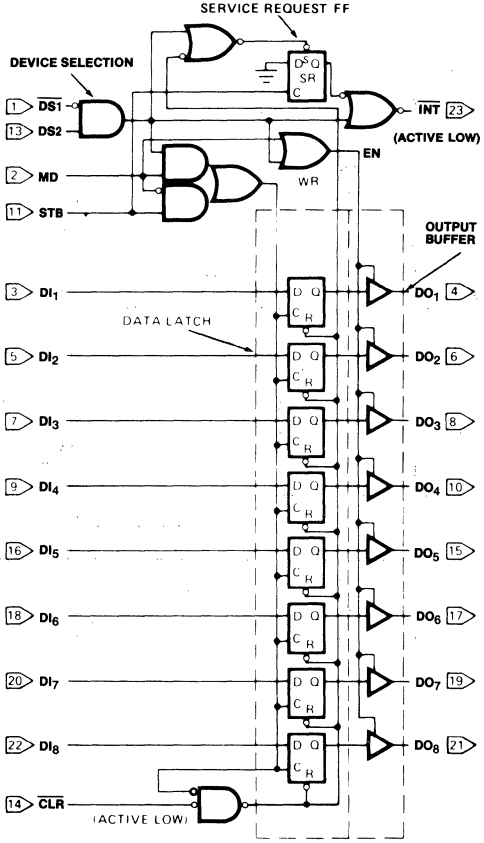
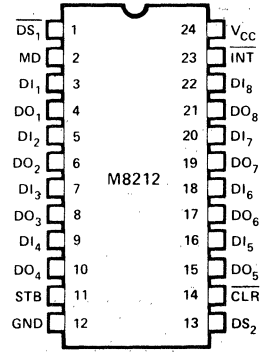


Figure 1. Logic Diagram



DI_1 DI_8	DATA IN
DO_1 DO_8	DATA OUT
$\overline{DS_1}$ $\overline{DS_2}$	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

Figure 2. Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +160°C
All Output or Supply Voltages .... −0.5 to +7 Volts
All Input Voltages ..... −1.0 to 5.5 Volts
Output Currents ..... 100 mA

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stess rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = +5V ±10%)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current STB, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current STB, DS, CR, DI_1-DI_8 Inputs			10	μA	V_R = V_{CC}
I_R	Input Leakage Current MD Input			30	μA	V_R = V_{CC}
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = V_{CC}
V_C	Input Forward Voltage Clamp			−1.2	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 10mA
V_{OH}	Output "High" Voltage	3.5	4.0		V	I_{OH} = -.5mA
I_{OS}	Short Circuit Output Current	-15		-75	mA	V_{CC} = 5.0V
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current		90	145	mA	

CAPACITANCE (F = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = + 5V, T_A = 25°C)

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	$\overline{DS_1}$ MD Input Capacitance	9 pF	15 pF
C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1-DI_8 Input Capacitance	5 pF	10 pF
C_{OUT}	DO -DO_8 Output Capacitance	8 pF	15 pF

Conditions of Test
Input Pulse Amplitude = 2.5V
Input Rise and Fall Times: 5 ns between 1V and 2V
Measurements made at 1.5V

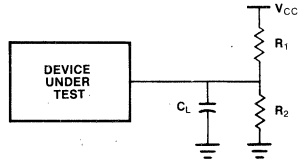
A.C. CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = +5V ±10%)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
t_{PW}	Pulse Width	40		ns	
t_{PD}	Data To Output Delay		30	ns	NOTE 1
t_{WE}	Write Enable To Output Delay		50	ns	NOTE 1
t_{SET}	Data Setup Time	20		ns	
t_H	Data Hold Time	30		ns	
t_R	Reset To Output Delay		55	ns	NOTE 1
t_S	Set To Output Delay		35	ns	NOTE 1
t_E	Output Enable/Disable Time		50	ns	NOTE 1 C_L = 30 pF
t_C	Clear To Output Delay		55	ns	NOTE 1

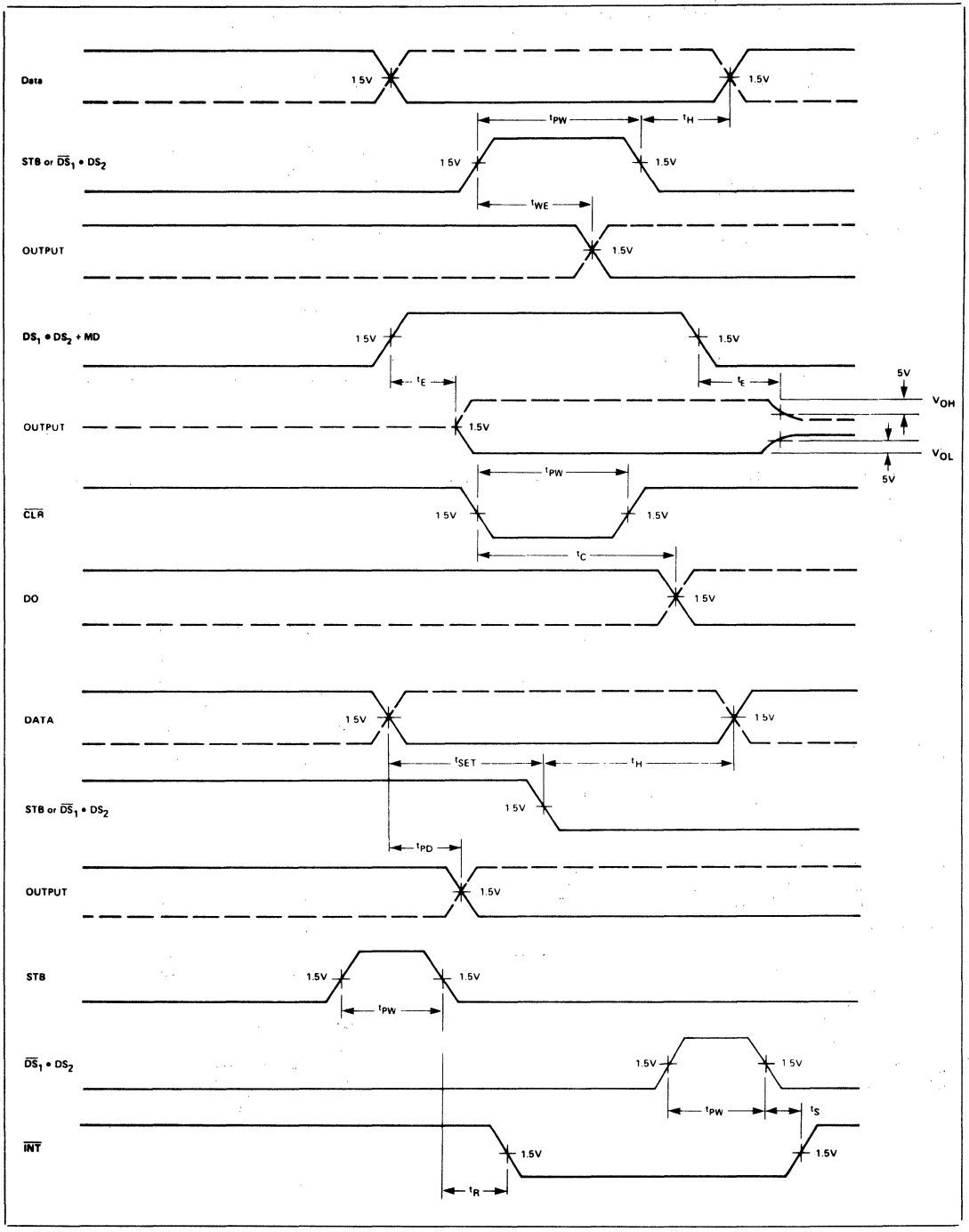
NOTE 1:

TEST	C_L	R_1	R_2
t_{PD}, t_{WE}, t_R, t_S, t_C	30pF	300Ω	600Ω
t_E, ENABLE↑	30pF	10KΩ	1KΩ
t_E, ENABLE↓	30pF	300Ω	600Ω
t_E, DISABLE↑	5pF	300Ω	600Ω
t_E, DISABLE↓	5pF	10KΩ	1KΩ

A.C. TESTING LOAD CIRCUIT



WAVEFORMS


Data
1.5V
1.5V
tPW
tH
STB or DS1 • DS2
1.5V
1.5V
tWE
OUTPUT
1.5V
DS1 • DS2 + MD
1.5V
1.5V
tE
tE
5V
VOH
OUTPUT
1.5V
VOL
5V
tPW
CLR
1.5V
1.5V
tC
DO
1.5V
DATA
1.5V
1.5V
tSET
tH
STB or DS1 • DS2
1.5V
tPD
OUTPUT
1.5V
STB
1.5V
1.5V
tPW
DS1 • DS2
1.5V
1.5V
tPW
tS
INT
1.5V
1.5V
tR