◢◤ National
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54F/74F412
Multi-Mode Buffered Latch with TRI-STATE® Outputs
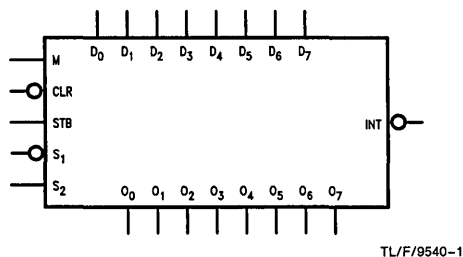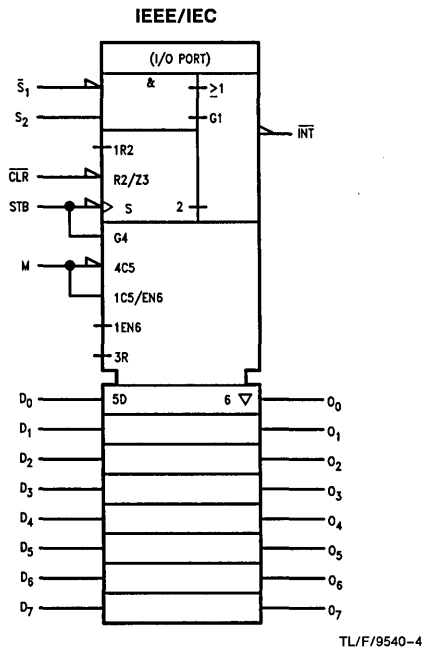
General Description

The 'F412 is an 8-bit latch with TRI-STATE output buffers. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode. The 'F412 is the functional equivalent of the Intel 8212.

Features

- TRI-STATE outputs
- Status flip-flop for interrupt commands
- Asynchronous or latched receiver modes
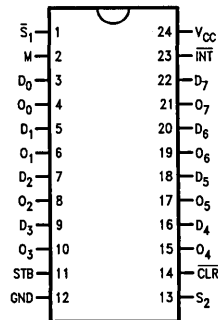- 300 mil 24-pin slim package
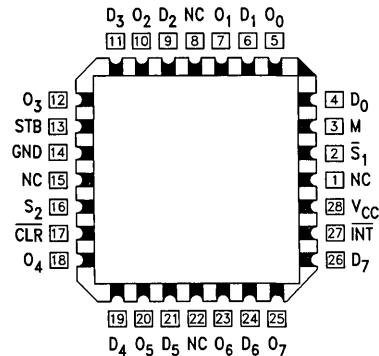
Ordering Code: See Section 5

Logic Symbols

IEEE/IEC

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Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak

$\bar{S}_1$	1		24	V_{CC}
M	2		23	$\overline{INT}$
D_0	3		22	D_7
O_0	4		21	O_7
D_1	5		20	D_6
O_1	6		19	O_6
D_2	7		18	D_5
O_2	8		17	O_5
D_3	9		16	D_4
O_3	10		15	O_4
STB	11		14	$\overline{CLR}$
GND	12		13	S_2

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Pin Assignment for LCC and PCC

D_3 O_2 D_2 NC O_1 D_1 O_0

D_4 O_5 D_5 NC O_6 D_6 O_7

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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
O_0–O_7	Latch Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)
D_0–D_7	Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{CLR}$	Clear	1.0/1.0	20 μA/−0.6 mA
STB	Strobe	1.0/1.0	20 μA/−0.6 mA
$\overline{INT}$	Interrupt	50/33.3	−1 mA/20 mA
M	Mode Control Input	1.0/1.0	20 μA/−0.6 mA
$\overline{S}_1$, S_2	Select Inputs	1.0/1.0	20 μA/−0.6 mA

Functional Description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The TRI-STATE data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is HIGH and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_1$ and S_2), and the strobe (STB) inputs and during transparency each data output (O_n) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M = L, the eight data latch inputs are enabled when the strobe is HIGH regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S}_1$ and S_2) inputs.

Data Latches Function Table

Function	$\overline{CLR}$	M	$\overline{S}_1$	S_2	STB	Data In	Data Out
Clear	L	H	H	X	X	X	L
	L	L	L	H	L	X	L
De-Select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	Q_0
	H	L	L	H	L	X	Q_0
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

Status Flip-Flop Function Table

$\overline{CLR}$	$\overline{S}_1$	S_2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	⌐	L
H	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Clock Transition

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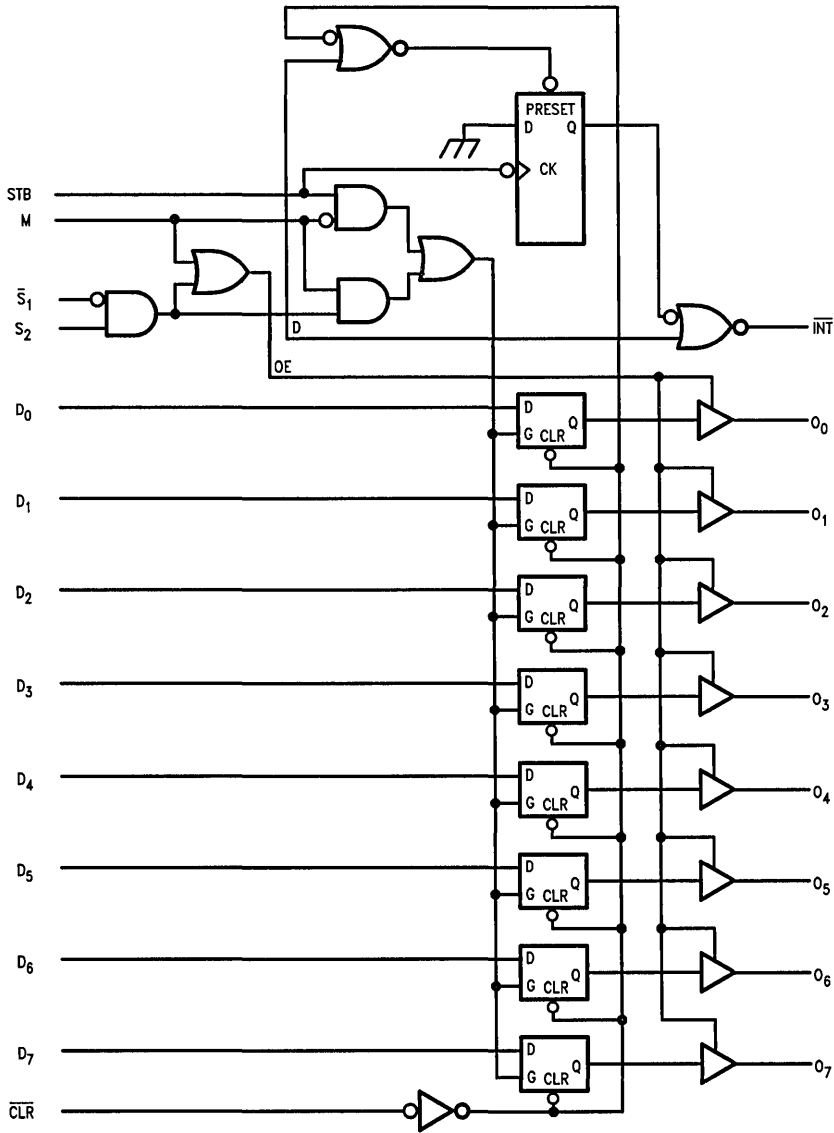
Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
Ambient Temperature under Bias	$-55°C$ to $+125°C$
Junction Temperature under Bias	$-55°C$ to $+175°C$

V_{CC} Pin Potential to
Ground Pin $\qquad$ $-0.5V$ to $+7.0V$

Input Voltage (Note 2) $\qquad$ $-0.5V$ to $+7.0V$

Input Current (Note 2) $\qquad$ -30 mA to $+5.0$ mA

Voltage Applied to Output
in HIGH State (with $V_{CC} = 0V$)
Standard Output $\qquad$ $-0.5V$ to V_{CC}
TRI-STATE Output $\qquad$ $-0.5V$ to $+5.5V$

Current Applied to Output
in LOW State (Max) $\qquad$ twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature
Military $\qquad$ $-55°C$ to $+125°C$
Commercial $\qquad$ $0°C$ to $+70°C$

Supply Voltage
Military $\qquad$ $+4.5V$ to $+5.5V$
Commercial $\qquad$ $+4.5V$ to $+5.5V$

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH	54F 10% V_{CC}	2.5					$I_{OH} = -1$ mA ($\overline{INT}$)
	Voltage	54F 10% V_{CC}	2.4					$I_{OH} = -3$ mA (O_n)
		74F 10% V_{CC}	2.5			V	Min	$I_{OH} = -1$ mA ($\overline{INT}$)
		74F 10% V_{CC}	2.4					$I_{OH} = -3$ mA (O_n)
		74F 5% V_{CC}	2.7					$I_{OH} = -1$ mA ($\overline{INT}$)
		74F 5% V_{CC}	2.7					$I_{OH} = -3$ mA (O_n)
V_{OL}	Output LOW	54F 10% V_{CC}			0.5			$I_{OL} = 20$ mA
	Voltage	74F 10% V_{CC}			0.5	V	Min	$I_{OL} = 20$ mA
		74F 10% V_{CC}			0.5			$I_{OL} = 24$ mA
I_{IH}	Input HIGH Current				20	μA	Max	$V_{IN} = 2.7V$
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	$V_{IN} = 7.0V$
I_{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
I_{OZH}	Output Leakage Current				50	μA	Max	$V_{OUT} = 2.7V$
I_{OZL}	Output Leakage Current				-50	μA	Max	$V_{OUT} = 0.5V$
I_{OS}	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	$V_{OUT} = V_{CC}$
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	$V_{OUT} = V_{CC}$
I_{CCH}	Power Supply Current			33	50	mA	Max	$V_O = $ HIGH
I_{CCL}	Power Supply Current			40	60	mA	Max	$V_O = $ LOW
I_{CCZ}	Power Supply Current			40	60	mA	Max	$V_O = $ HIGH Z

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AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F $T_A, V_{CC} = $ Mil $C_L = 50$ pF		74F $T_A, V_{CC} = $ Com $C_L = 50$ pF		Units	Fig No
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	3.5 2.5	6.5 5.0	8.5 6.5	3.0 2.0	11.5 8.5	3.0 2.0	9.5 7.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_1$, S_2 or STB to O_n	8.5 7.5	14.5 12.5	18.5 16.0	6.5 6.0	23.0 19.0	7.5 6.5	20.5 17.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_1$ or S_2 to $\overline{INT}$	4.5 4.5	7.5 8.0	9.5 10.5	3.5 3.5	12.0 12.5	4.0 4.0	10.5 11.5	ns	2–3
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	7.5	12.5	16.0	5.5	18.5	6.5	17.5	ns	2–3
t_{PHL}	Propagation Delay STB to $\overline{INT}$	6.5	11.0	14.0	5.5	17.5	5.5	15.0	ns	2–3
t_{PZH} t_{PZL}	Access Time, HIGH or LOW $\overline{S}_1$ to O_n	8.0 6.5	12.5 11.0	18.0 14.0	6.5 5.5	20.0 18.0	7.0 5.5	19.0 15.0	ns	2–5
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW $\overline{S}_1$ to O_n	4.5 6.5	8.0 11.0	10.5 14.0	4.0 5.5	14.5 17.0	4.0 5.5	11.5 15.0	ns	2–5
t_{PZH} t_{PZL}	Access Time, HIGH or LOW S_2 to O_n	7.5 5.0	12.5 9.0	16.0 11.5	6.5 4.0	18.5 15.5	6.5 4.5	17.5 12.5	ns	2–5
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW S_2 to O_n	4.5 5.5	7.5 9.5	9.5 12.0	3.5 4.5	12.5 14.5	4.0 4.5	10.5 13.0	ns	2–5
t_{PZH} t_{PZL}	Access Time, HIGH or LOW M to O_n	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.0	16.0 15.0	4.5 4.5	12.0 12.0	ns	2–5
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW M to O_n	4.0 5.0	7.0 8.5	9.0 11.0	3.5 4.5	11.5 14.0	3.5 4.5	10.0 12.0	ns	2–5

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = $ Mil		74F $T_A, V_{CC} = $ Com		Units	Fig No
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{S}_1$, S_2 or STB	0 0		2.0 2.0		1.0 1.0		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time D_n to $\overline{S}_1$, S_2 or STB	8.0 8.0		10.0 10.0		9.0 9.0		ns	2–6
$t_w(H)$ $t_w(L)$	$\overline{S}_1$, S_2 or STB Pulse Width, HIGH or LOW	8.0 8.0		11.0 11.0		9.0 9.0		ns	2–4
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	8.0		11.5		9.0		ns	2–4