National Semiconductor

54F/74F432
Multi-Mode Buffered Latch with TRI-STATE® Outputs

General Description

The 'F432 is an 8-bit latch with TRI-STATE output buffers and control and device selection logic. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode.

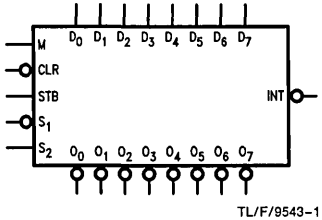
The 'F432 is the functional equivalent of the Intel 8212, but with inverting outputs.

Features

- TRI-STATE inverting outputs
- Status flip-flop for interrupt commands
- Asynchronous or latched receiver modes
- Data to output propagation delay typically 8.5 ns
- Supply current 43 mA typ
- 24-pin slim package

Ordering Code: See Section 5

Logic Symbols



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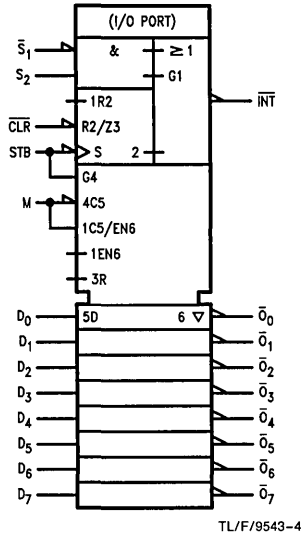
IEEE/IEC



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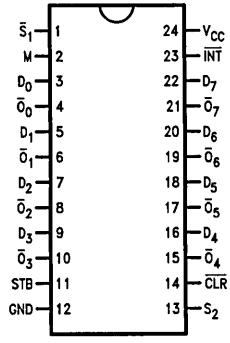
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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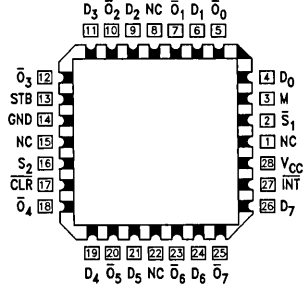
Pin Assignment for LCC and PCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_7	Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{O}_0$–$\overline{O}_7$	Latch Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)
$\overline{S}_1$,–$\overline{S}_2$,	Select Inputs	1.0/1.0	20 μA/−0.6 mA
M	Mode Control Input	1.0/1.0	20 μA/−0.6 mA
STB	Strobe	1.0/1.0	20 μA/−0.6 mA
$\overline{INT}$	Interrupt	50/33.3	−1 mA/20 mA
$\overline{CLR}$	Clear	1.0/1.0	20 μA/−0.6 mA

Functional Description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The TRI-STATE data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is HIGH and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_1$ and S_2), and the strobe (STB) inputs and during transparency each data output ($\overline{O}_n$) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches. See Data Latches Function Table.

An input mode or an output mode is selectable from this single input line. In the input mode, M = L, the eight data latch inputs are enabled when the strobe is HIGH regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW the latches will store the most recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S}_1$ and S_2) inputs. See Data Latches Function Table.

Data Latches Function Table

Function	$\overline{CLR}$	M	$\overline{S}_1$	S_2	STB	Data In	Data Out
Clear	L	H	H	X	X	X	H
	L	L	L	H	L	X	H
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	$\overline{Q}_0$
	H	L	L	H	L	X	$\overline{Q}_0$
Data Bus	H	H	L	H	X	L	H
	H	H	L	H	X	H	L
Data Bus	H	L	L	H	H	L	H
	H	L	L	H	H	H	L

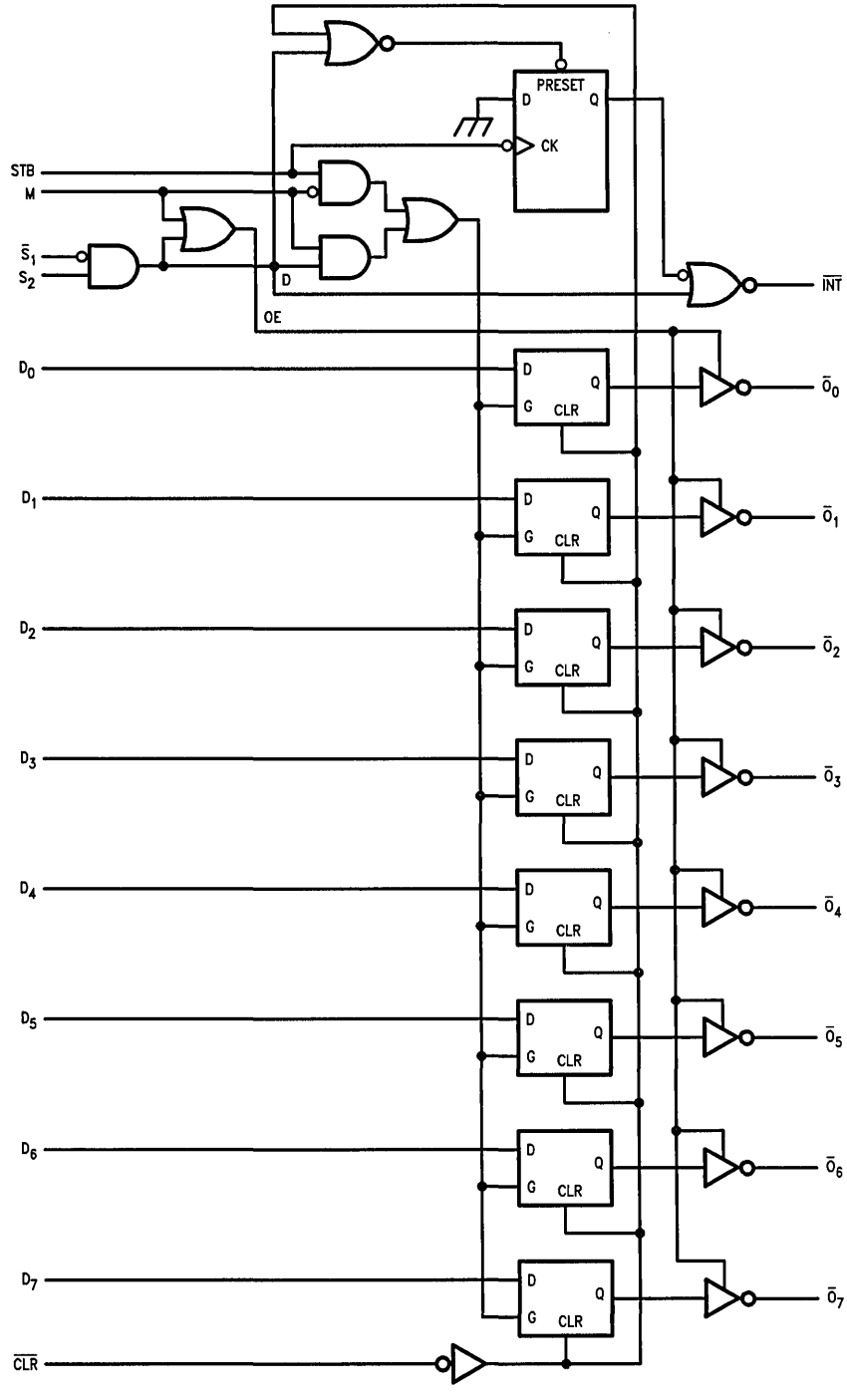
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Status Flip-Flop Function Table

$\overline{CLR}$	$\overline{S}_1$	S_2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↗	L
H	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA
I_{IH}	Input HIGH Current				20	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				1.0	mA	Max	V_{IN} = 5.5V
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = V_{CC}
I_{CCH}	Power Supply Current			50	65	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			50	65	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			50	65	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig No
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	3.5 2.5	8.5 5.5	10.5 7.0			3.0 3.0	12.0 12.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_1$, S_2 or STB to $\overline{O}_n$	8.5 6.5	16.0 12.5	21.0 16.0			7.5 5.5	23.0 18.0	ns	2-3
t_{PHL}	Propagation Delay $\overline{CLR}$ to $\overline{O}_n$	7.0	15.0	18.5			6.0	20.5	ns	2-3
t_{PHL}	Propagation Delay STB to $\overline{INT}$	6.0	11.5	14.5			5.0	16.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_1$ to $\overline{INT}$	4.0 5.5	7.5 7.5	9.5 12.0			3.5 5.5	10.5 13.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay S_2 to $\overline{INT}$	4.0 4.5	7.5 7.5	9.5 9.5			3.5 4.5	10.5 10.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay M to $\overline{O}_n$	9.0 6.5	15.0 11.0	19.0 14.0			9.0 6.5	20.0 15.0	ns	2-3
t_{PZH} t_{PZL}	Enable Time M to $\overline{O}_n$	6.0 6.0	8.5 8.5	14.0 13.0			6.0 6.0	15.0 14.5	ns	2-5
t_{PHZ} t_{PLZ}	Disable Time M to $\overline{O}_n$	4.5 5.5	6.5 9.5	9.5 12.0			4.5 5.5	10.5 13.0	ns	2-5
t_{PZH} t_{PZL}	Enable Time $\overline{S}_1$, S_2 to $\overline{O}_n$	4.5 5.0	13.0 11.0	18.0 15.0			4.0 4.0	20.0 17.0	ns	2-5
t_{PHZ} t_{PLZ}	Disable Time $\overline{S}_1$, S_2 to $\overline{O}_n$	4.0 5.0	8.0 11.0	11.0 15.5			3.5 4.0	12.5 17.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig No
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{S}_1$ to D_n	0 0				0 0		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{S}_1$ to D_n	11.0 8.5				12.5 9.5			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S_2 to D_n	0 0				0 0		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_2 to D_n	9.0 7.0				9.0 7.0		ns	2–6
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW STB to D_n	0 0				0 0		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW STB to D_n	13.0 10.0				13.0 10.0		ns	2–6
$t_w(H)$ $t_w(L)$	STB Pulse Width HIGH or LOW	5.0 5.0				5.0 5.0		ns	2–4
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	10.0				10.0		ns	2–4
$t_w(H)$ $t_w(L)$	$\overline{S}_1$ Pulse Width HIGH or LOW	9.0 7.0				9.0 7.0		ns	2–4
$t_w(H)$ $t_w(L)$	S_2 Pulse Width HIGH or LOW	7.0 9.0				7.0 9.0		ns	2–4