National Semiconductor

APRIL 1978

INS8212 8-Bit Input/Output Port

General Description

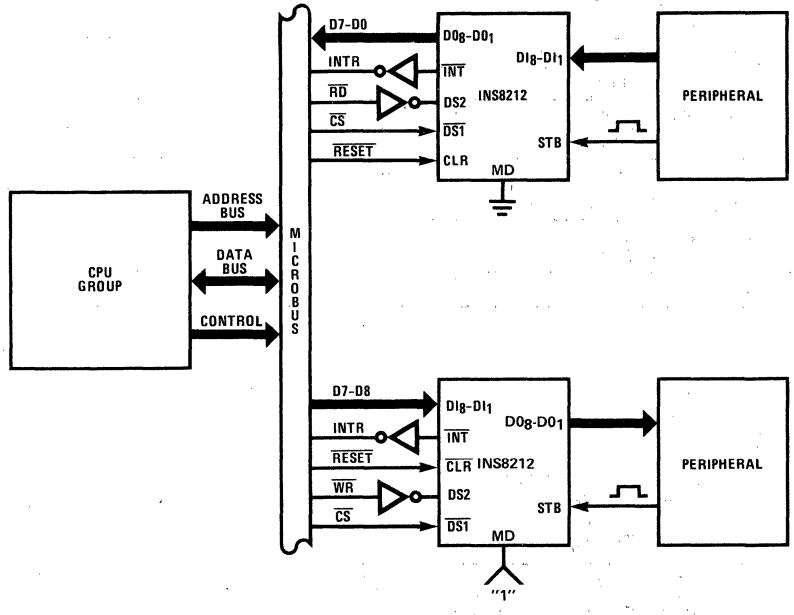
The INS8212 is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's INS8080A microprocessor family. The INS8212 can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The INS8212 includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

Features

- 8-Bit Data Latch and Buffer
- Service Request Flip-Flop for Generation and Control of Interrupts
- 0.25 mA Input Load Current
- TRI-STATE TTL Output Drive Capability
- Outputs Sink 15 mA
- Asynchronous Latch Clear
- 3.65V Output for Direct Interface to INS8080A
- Reduces System Package Count by Replacing Buffers, Latches, and Multiplexers in Microcomputer Systems
- MICROBUS™* Compatible

INS8212 MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings

Temperature Under Bias Plastic . . . . . −65°C to +75°C
Storage Temperature . . . . . −65°C to +160°C
All Output or Supply Voltages. . . . . −0.5V to +7V
All Input Voltages. . . . . −1.0V to 5.5V
Output Currents 125mA

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

$T_A = 0°C$ to $+75°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current STB, DS_2, $\overline{CLR}$, DI_1-DI_8 Inputs			−0.25	mA	$V_F = 0.45V$
I_F	Input Load Current MD Input			−0.75	mA	$V_F = 0.45V$
I_F	Input Load Current $\overline{DS_1}$ Input			−1.0	mA	$V_F = 0.45V$
I_R	Input Leakage Current STB, DS_2, $\overline{CLR}$, DI_1-DI_8 Inputs			10	μA	$V_R = 5.25V$
I_R	Input Leakage Current MD Input			30	μA	$V_R = 5.25V$
I_R	Input Leakage Current $\overline{DS_1}$ Input			40	μA	$V_R = 5.25V$
V_C	Input Forward Voltage Clamp			−1	V	$I_C = -5mA$
V_{IL}	Input "Low" Voltage			0.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			0.45	V	$I_{OL} = 15mA$
V_{OH}	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1mA$
I_{SC}	Short Circuit Output Current	−15		−75	mA	$V_O = 0V$
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	$V_O = 0.45V/5.25V$
I_{CC}	Power Supply Current		90	130	mA	

Capacitance*

$F = 1MHz$, $V_{BIAS} = 2.5V$, $V_{CC} = +5V$, $T_A = 25°C$

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	DS_1, MD Input Capacitance	9pF	12pF
C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1-DI_8 Input Capacitance	5pF	9pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8pF	12pF

*This parameter is sampled and not 100% tested.

AC Electrical Characteristics

$T_A = 0°C$ to $+75°C$, $V_{CC} = +5V \pm 5\%$

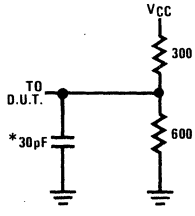
Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{PW}	Pulse Width	30			ns	
t_{PD}	Data to Output Delay			30	ns	
t_{WE}	Write Enable to Output Delay			40	ns	
t_{SET}	Data Setup Time	15			ns	
t_H	Data Hold Time	20			ns	
t_R	Reset to Output Delay			40	ns	
t_S	Set to Output Delay			30	ns	
t_E	Output Enable/Disable Time			45	ns	
t_C	Clear to Output Delay			55	ns	

Switching Characteristics

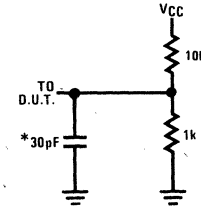
Conditions of Test:

1. Input Pulse Amplitude = 2.5V.
2. Input Rise and Fall Times = 5ns.
3. Between 1V and 2V Measurements made at 1.5V with 15mA & 30pF Test Load.

Test Load
15mA & 30pF



Alternate Test Load



*including jig & probe capacitance

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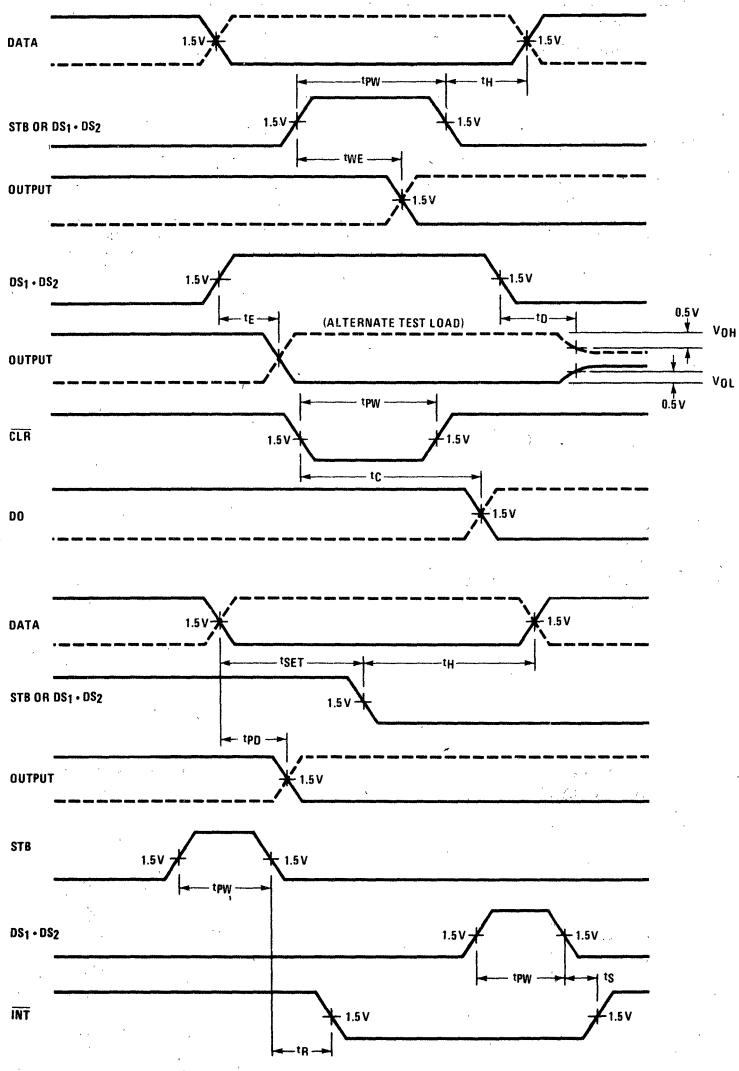
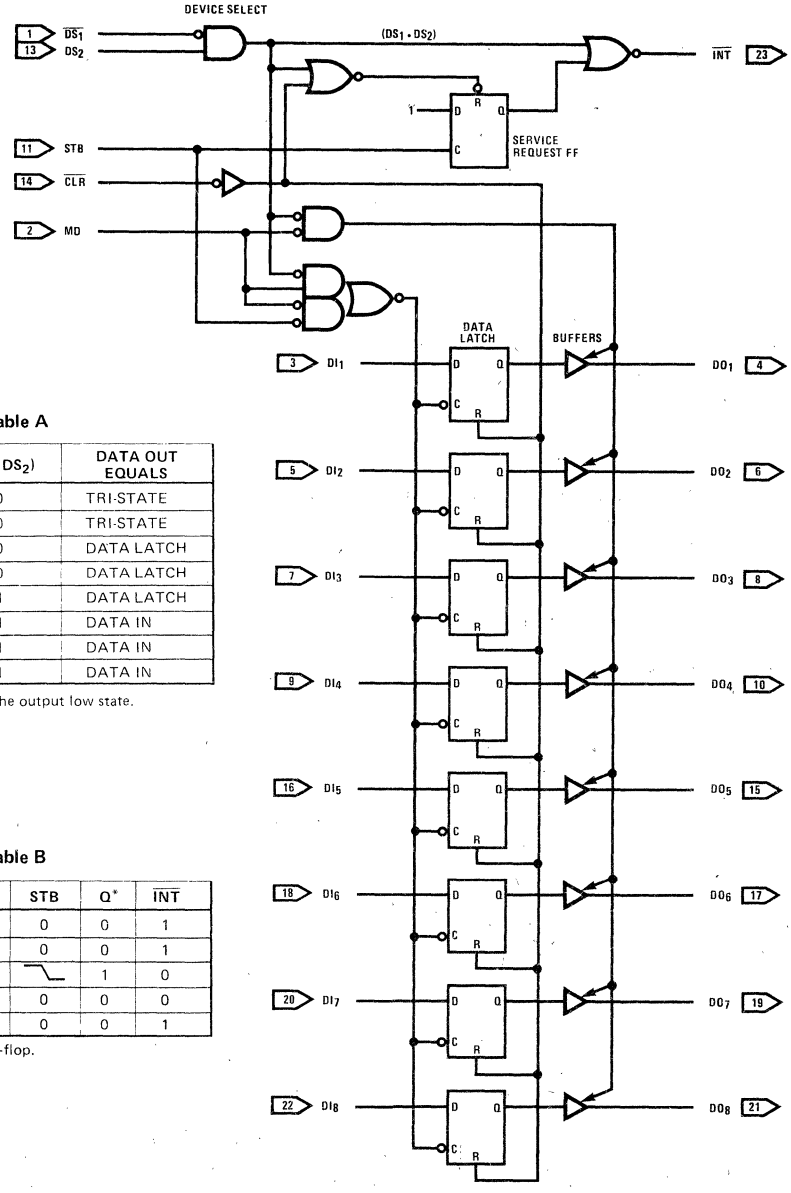
Timing Diagram



INS8212 Logic Diagram



Logic Table A

STB	MD	$(DS_1 \cdot DS_2)$	DATA OUT EQUALS
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ ⌥ resets data latch to the output low state.

Logic Table B

$\overline{CLR}$	$(DS_1 \cdot DS_2)$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌥	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

INS8212 Functional Pin Definitions

The following describes the function of all the INS8212 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select (DS_1, DS_2): When DS_1 is low and DS_2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic $(DS_1 \cdot DS_2)$. When low (input mode), the state of the output buffers is determined by the device selection logic $(DS_1 \cdot DS_2)$ and the source of the data latch clock input is the strobe (STB) input.

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INS8212 Functional Pin Definitions continued

Strobe (STB): Used as data latch clock input when the mode (MD) input is low (input mode). Also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In (DI_1-DI_8): Eight-bit data input to the data latch, which consists of eight D-type flip-flops. While the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. The clock input high overrides the clear (CLR) input data latch reset.

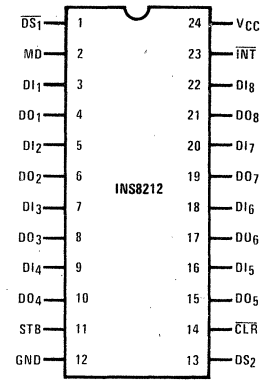
Clear (CLR): When low, asynchronously resets (clears) the data latch and the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

OUTPUT SIGNALS

Interrupt (INT): Goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

Data Out (DO_1-DO_8): Eight-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

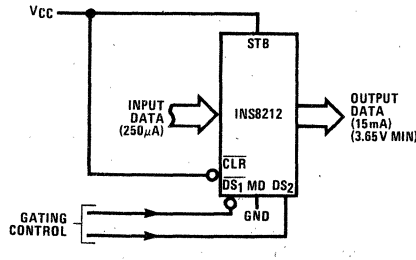
Pin Configuration



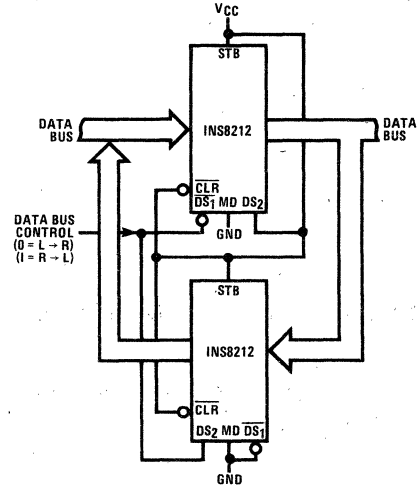
NOTE: INS8212 Identical to DP8212

Applications in Microcomputer Systems

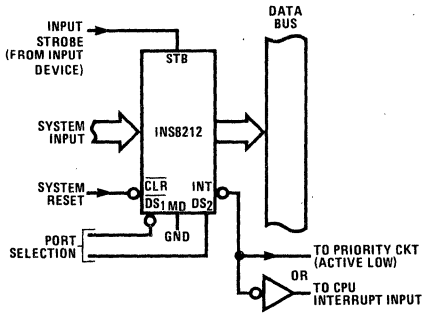
Gated Buffer
(TRI-STATE)



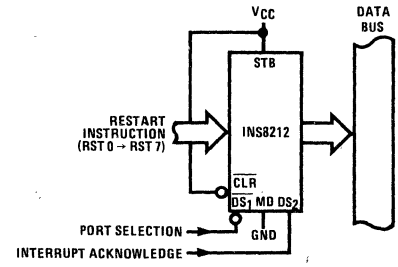
Bidirectional Bus Driver



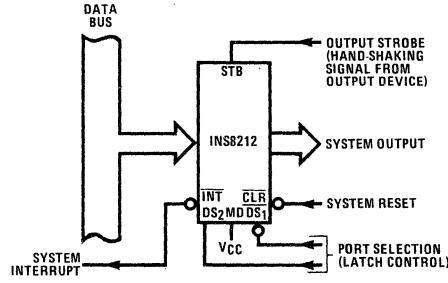
Interrupting Input Port



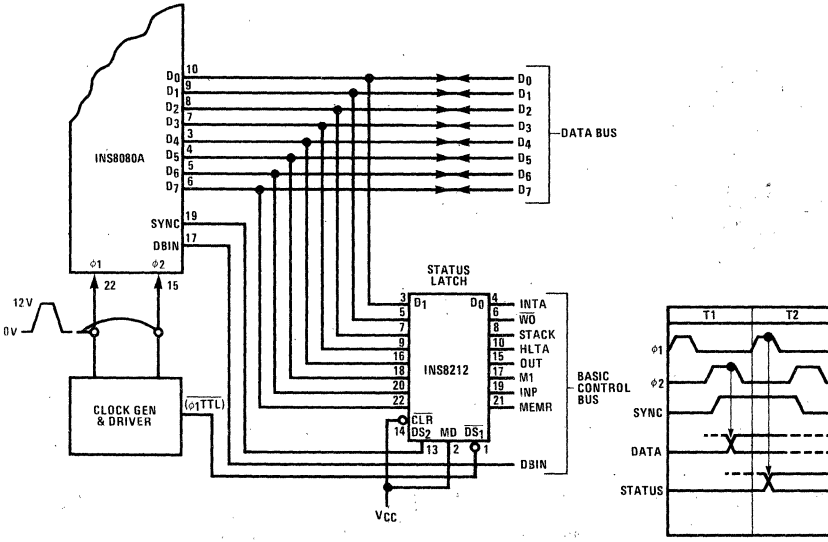
Interrupt Instruction Port



Output Port (with Hand-Shaking)



INS8080A Status Latch



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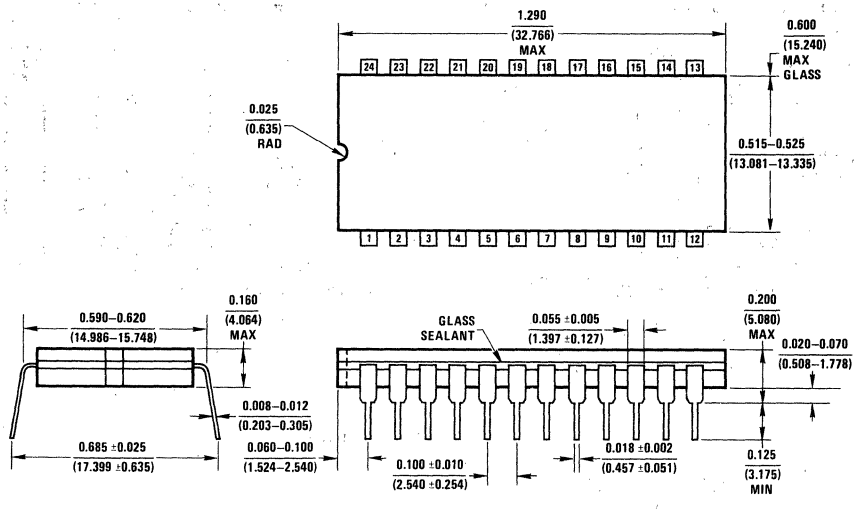
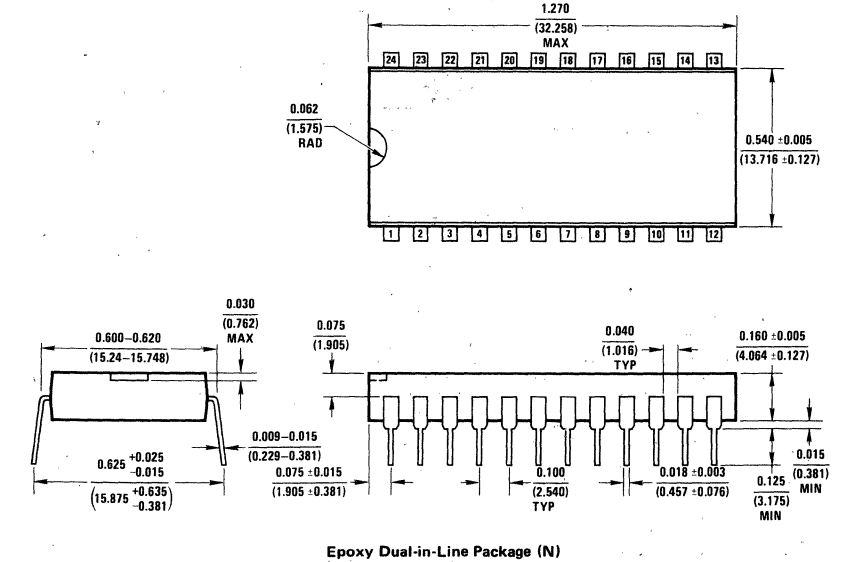
Physical Dimensions



Ceramic Dual-in-Line Package (J)
Order Number INS8212J



Epoxy Dual-in-Line Package (N)
Order Number INS8212N

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